TIPS FOR DESIGNING HIGH-GAIN AMPLIFIERS

TRANSISTOR MODELS, ENGINEERING APPROXIMATIONS, AND GAIN AND BANDWIDTH CALCULATIONS HELP SIMPLIFY AMPLIFIER DESIGN.

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Several techniques that emphasize intuition, not analytical results, can help simplify the design of a high-gain amplifier with wide bandwidth. This article takes a look these techniques, which include transistor models, gain and bandwidth calculations, and engineering approximations. The outcome is convincing—an augmented transistor model and a few back-of-the-envelope calculations yield surprisingly predictable results. Also presented here is a practical example and a discussion of design strategy.

Suppose you need to design a transistor amplifier with −1000 gain and a 1-MHz, −3-dB bandwidth. An op amp isn't available, and you want to do the design with as few components as possible. An amplifier circuit is submitted for your approval *(Fig. 1a)*. Will it do the job?

The small-signal network for this common-emitter amplifier is drawn using the standard transistor hybrid-π model *(Fig. 1b)*. The mid-band gain of this amplifier is:

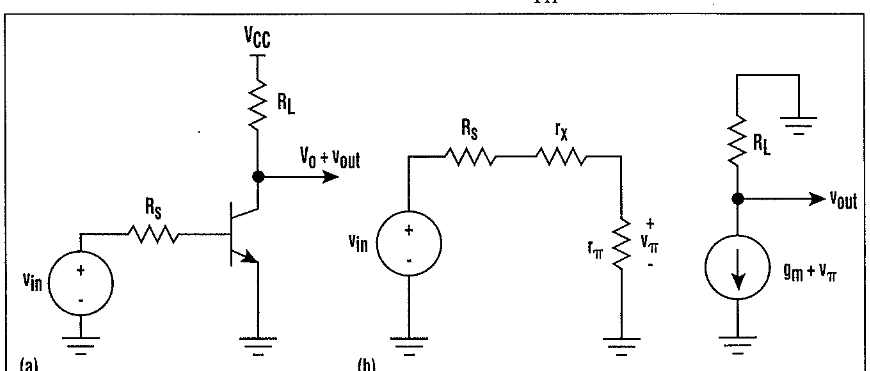
$$\frac{v_{out}}{v_{in}} = -g_m R_L \frac{r_\pi}{R_s + r_x + r_\pi} \qquad (1)$$

The gain of this amplifier approaches a theoretical maximum when R_s and r_x are small compared to r_π.

$$\frac{v_{out}}{v_{in}} \approx -g_m R_L \qquad (2)$$

Equation 2 calculates the maximum gain achievable with one resistively-loaded gain stage. From transistor theory, we know that the transconductance of a transistor is linearly proportional to collector current:

$$g_m = \frac{I_c}{V_{TH}} \qquad (3)$$



1. A RESISTIVELY-LOADED common-emitter amplifier is used as a high-gain circuit (a). The small-signal network for this common-emitter amplifier is drawn using the standard transistor hybrid-π model (b).

DESIGNING HIGH-GAIN AMPLIFIERS

where the transistor thermal voltage $V_{TH} = kT/q \approx 25$ mV at room temperature. The small-signal gain is:

$$\frac{v_{out}}{v_{in}} \approx -\frac{I_C}{V_{TH}} R_L \qquad (4)$$

For the transistor to stay biased in its linear region, the quiescent output voltage V_o must be higher than ground. The collector current of the transistor amplifier depends on power-supply voltage V_{CC} and quiescent output voltage:

$$I_C = \frac{V_{CC} - V_o}{R_L} \qquad (5)$$

Finally, this gives a maximum theoretical gain of:

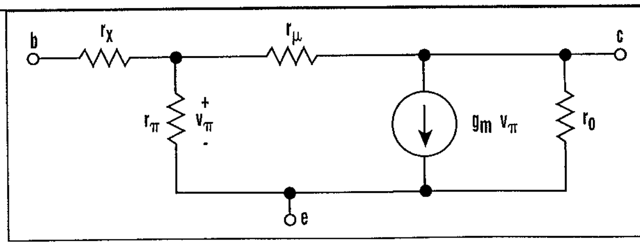
$$\frac{v_{out}}{v_{in}} \approx -\frac{(V_{CC} - V_o)}{V_{TH}} \qquad (6)$$

For a supply voltage of 12 V and a small V_o, this transistor model shows that the small signal gain always will be less than 480. And if a reasonable output swing is desired, the gain will be significantly lower.

The simple hybrid-π model used for this analysis indicates that the voltage gain of a resistively-loaded amplifier may be increased to ∞ by increasing the power-supply voltage. Alternately, if the transistor is loaded with an ideal current source ($R_L = \infty$), the model shows that we can get infinite voltage gain. But common sense prevails and a more detailed look at the inner workings of the transistor reveals that infinite gain is impossible. We then must modify the hybrid-π model for high-gain circuits.

DETAILED MODEL

The simple hybrid-π model leads us to believe that transistor collector current doesn't change when collector voltage changes.[1] In other words, the simple model indicates infinite output impedance at a transistor's collector. Looking at an I_C versus V_{CE} trace on a transistor curve tracer dispels this notion. James Early was the first to describe this effect, called base-width modulation.[2].



2. MORE DETAIL is given to the simple hybrid-π transistor model by adding two more resistors to account for the effects of base-width modulation.

Base-width modulation causes both the collector current and base current of the transistor to change when the collector voltage changes. This also means that a transistor current source can't have infinite output impedance. The effect is modeled by adding two more resistors to the transistor model *(Fig. 2)*. This augmented low-frequency model should be used when analyzing circuits with gains in excess of a few hundred.

The g_m and r_π for the extended model are the same as before:

$$g_m \approx \frac{I_C}{V_{TH}} \qquad (7)$$

$$r_\pi = \frac{h_{fe}}{g_m} \qquad (8)$$

As a result of base-width modulation, the output resistance of the transistor (r_o) is inversely proportional to collector current.

$$r_o = \frac{1}{\eta g_m} \qquad (9)$$

The proportionality constant η is what device physicists call the base-width modulation factor, which has typical values of 10^{-3} to 10^{-4}.

A change in collector voltage also affects base current. Changes in base current are a factor of h_{fe} smaller than changes in collector current. Therefore, the feedback resistance r_μ is:

$$r_\mu = h_{fe} r_o \qquad (10)$$

The picture gets clearer by plugging some real numbers into the equations. Using a curve tracer, the output resistance r_o and small-signal current gain h_{fe} of four 2N3904 and 2N3906 transistors were measured (surely not a scientific sampling, but who cares?). Other averaged parameters (r_π, g_m, r_μ) were calculated *(Table 1)*. The averaged transistor-model values will be used to design a high-gain transistor amplifier.

A DESIGN EXAMPLE

Consider the design of a one-gain-stage amplifier *(Table 2)*. A common-emitter amplifier loaded with a current source will be designed using the measured transistor data *(Fig. 3a)*.

Q_1 is the common-emitter amplifier, loaded with current-source transistor Q_2. The current source has a high output resistance, resulting in high gain from this one stage. The value of the input coupling capacitor is chosen C_c to meet the f_L specification.[3] Q_1 and Q_2 are biased at approximately 2.5 mA.

Q_3 buffers the output, and Q_4 is a V_{BE}-multiplier providing a voltage drop of approximately 8 V_{BE} so that the feedback loop will bias the transistors properly. Ignoring the loading effects of $r_{\pi 1}$ on R_{in} and R_f, the amplifier's closed-loop gain is set by varying the potentiometer setting. Closed-loop gain is approximately given by:

$$\frac{v_{out}}{v_{in}} \approx -\frac{R_f}{R_{in}} \qquad (11)$$

This gain equation is exactly like that of an inverting op-amp gain stage. In order for the amplifier to behave like an "ideal" amplifier, and for the gain equation to hold true, the amplifier's open-loop gain must be much larger than 1000. So, let's figure out the open-loop gain *(Fig. 3b)*.

Several approximations can be made when calculating open-loop gain. First, $r_\pi > R_{in}$, so the transistor's

TABLE 1: AVERAGE TRANSISTOR PARAMETERS

Transistor	I_c	r_π	g_m	r_o	h_{fe}	r_μ
2N3904	5 mA	1 kΩ	0.2 mho	75 kΩ	200	15 MΩ
2N3906	5 mA	875 Ω	0.2 mho	27 kΩ	175	4.7 MΩ

TABLE 2: DESIGN SPECIFICATIONS

Transistors	2N3904, 2N3906
Gain	> 1000
f_L (low-frequency –3-dB point)	< 500 Hz
f_H (high-frequency –3-dB point)	> 1 MHz
Power dissipation	< 100 mW
Power-supply voltages	+12, –12

TABLE 3: TRANSISTOR SMALL-SIGNAL PARAMETERS

Transistor	I_c	g_m	r_π	r_o	r_μ	C_π	C_μ
Q_1	2.5 mA	0.1	2 kΩ	150 kΩ	30 MΩ	50 pF	2 pF
Q_2	2.5 mA	0.1	1.75 kΩ	54 kΩ	9.4 MΩ	50 pF	4 pF
Q_3	1.5 mA	0.06	3.33 kΩ	250 kΩ	50 MΩ	30 pF	2 pF
Q_5	2.5 mA	0.1	2 kΩ	150 kΩ	30 MΩ	50 pF	3 pF

TABLE 4: TRY 1—CURRENT-SOURCE-LOADED COMMON-EMITTER AMPLIFIER

Parameter	Spice results	Prototype measurements
Closed-loop gain	1070	1050
f_L	180 Hz	190 Hz
f_H	220 kHz	400 kHz
Output swing	5 V p-p	5 V p-p
Power dissipation	70 mW	75 mW

input impedance won't load down the input that much. Second, the effective resistance due to feedback is R_f /(open-loop gain). This is also much smaller than R_{in}. The current-source transistor Q_2 is replaced by an equivalent resistance r_{out2} looking into the collector of Q_2. (We'll figure out real numbers later.) The emitter follower is replaced by an equivalent input resistance r_{in3} looking into the base of Q_3. Furthermore, the gain of the emitter follower will be close to 1, and won't be calculated here. The amplifier's open-loop gain is solved by summing currents at the output node:

$$g_{m1}v_{in} + \frac{v_{out}}{r_{o1}\|r_{out2}\|r_{in3}} + \frac{v_{out} - v_{in}}{r_{\mu1}} = 0 \qquad (12)$$

By grouping terms, and making the approximations:

$$g_{m1} >> \frac{1}{r_{\mu1}},\ r_{\mu1} >> r_{o1} \qquad (13)$$

we arrive at the final answer:

$$\frac{v_{out}}{v_{in}}(\text{open loop}) \approx -g_{m1}\{r_{o1}\|r_{out2}\|r_{in3}\} \qquad (14)$$

This is similar to the gain equation for the resistively-loaded common-emitter amplifier, except that in this case the load resistance at the output node has been made quite large by using a current source. Also, we can't ignore the input impedance of the emitter follower and the output resistance of Q_1. Going by the data in Table 1, we know that r_{o1} for Q_1 is approximately 150 kΩ, because r_o is inversely proportional to collector current, and Q_1 is biased at 2.5 mA. We still need to calculate the output resistance of the Q_2 current source r_{out2}, and the input resistance r_{in3} of the Q_3 emitter follower.

Q_1 and Q_2 are biased at 2.5 mA, with Q_3 biased at approximately 1.5 mA. The f_T for the 2N3904 and 2N3906 transistors is about 300 MHz. Each transistor has a base-spreading resistance $r_x \approx 150\ \Omega$ at this bias level. The C_π of each transistor is calculated by:

$$C_\pi \approx \frac{g_m}{2\pi f_T} - C_\mu \qquad (15)$$

C_μ for each transistor is a few picofarads, and depends somewhat on the collector-base voltage. Small-signal parameters can be calculated for these bias levels *(Table 3)*.

We'll use a small-signal model to

THE MILLER APPROXIMATION

The Miller approximation is a useful way to think about high-gain amplifiers. For the common-emitter amplifier, consider the small-signal model *(see the figure, a)*. The amplifier is driven by a voltage source with source resistance R'_s, which may include the base-spreading resistance r_x of the transistor. Capacitance at node v_a may be modeled as C_π in parallel with some other elements. Then, the mid-band gain is:

$$\frac{v_{out}}{v_a} \approx -g_m R_L \qquad (B1)$$

The feedback around C_μ can be modeled with $a_v = g_m R_L$ as the gain from base to collector *(see the figure, b)*. The capacitance looking to the right of C_π is the so-called Miller capacitance. Miller capacitance is found by applying a test-voltage source to the v_a node, and finding the test current.

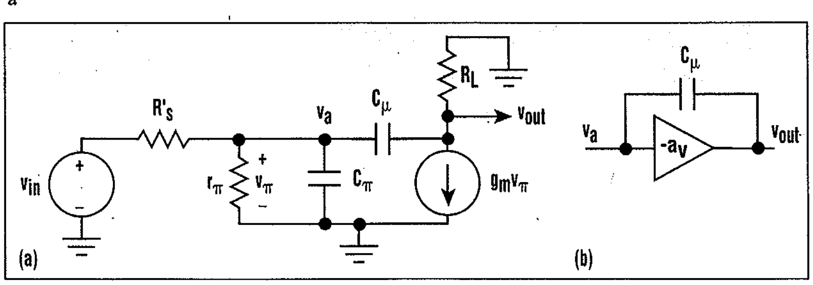
$$C_M = (1 + a_v)C_\mu \qquad (B2)$$

Total capacitance at node v_a is the sum of the Miller capacitance C_M with the intrinsic transistor capacitance C_π:

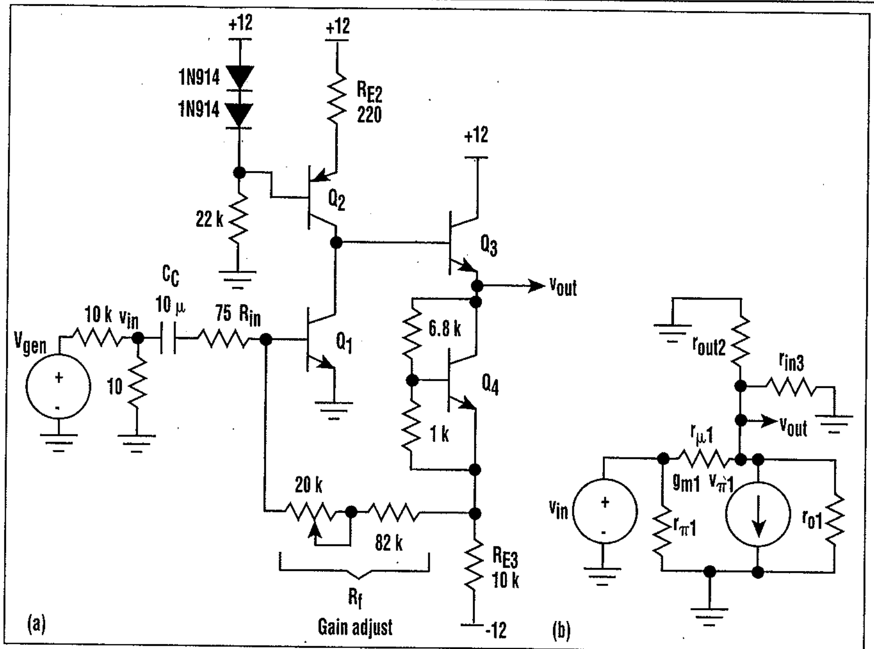
$$C_{in} \approx C_\pi + (1 + a_v)C_\mu \qquad (B3)$$

For a high-gain amplifier ($g_m R_L$ is large), the input capacitance is often dominated by the Miller capacitance, which is proportional to amplifier gain. In this high-gain case, the bandwidth of the amplifier is approximately given by the following equation:

$$\omega_h \approx \frac{1}{(R'_s\|r_\pi)C_{in}} \qquad (B4)$$



An exact analysis shows that the Miller-effect approximation is equivalent to calculating the dominant pole of the amplifier and ignoring other poles. In many cases, amplifier poles are widely spaced with one dominant pole, so it turns out that the approximation is a very good one.



3. A ONE-GAIN-STAGE common-emitter amplifier loaded with a current source is designed using the measured transistor data (a). The amplifier's open-loop gain is calculated from the circuit's small-signal model (b).

find the output resistance of the current source Q_2 *(Fig. 4a)*. A simplifying approximation is to ignore r_{x2} (which is small compared to $r_{\pi2}$) and the resistance of the diode string that's biasing Q_2's base (which is also small). To find this output resistance, add a test-voltage source V_T, and calculate the resulting current I_T.

At first, this circuit looks complicated, but it can be simplified to ease the calculation. It's clear from Figure 4 that the resistance at the collector of Q_2 is $r_{\mu2}$ in parallel with a bunch of other elements. Let's omit $r_{\mu2}$ and add it in later. We'll first find the output resistance of the modified circuit *(Fig. 4b)*.

Because the entire test current flows through the r_π-R_{E2} combination, the voltage $v_{\pi2}$ is found by:

$$v_{\pi2} = -I_T(r_{\pi2} \| R_{E2}) \quad (16)$$

where R_{E2} is the 220-Ω resistor at the emitter of Q_2. Solving for the test current:

$$I_T = \frac{V_T + v_{\pi2}}{r_{o2}} + g_{m2}v_{\pi2} = \frac{V_T - I_T(r_{\pi2} \| R_{E2})}{r_{o2}} - g_{m2}I_T(r_{\pi2} \| R_{E2}) \quad (17)$$

Recognizing that $g_{m2} > 1/r_{o2}$, this reduces to:

$$I_T\{1 + g_{m2}(r_{\pi2} \| R_{E2})\} \approx \frac{V_T}{r_o} \quad (18)$$

Now, adding in the $r_{\mu2}$, which we previously omitted, results in:

$$r_{out2} \approx r_{\mu2} \| r_o\{1 + g_{m2}(r_{\pi2} \| R_{E2})\} \quad (19)$$

TABLE 5: TRY 2—CURRENT-SOURCE-LOADED COMMON-EMITTER AMPLIFIER (WITH CASCODE)

Parameter	Spice results	Prototype measurements
Gain	1110	1100
f_L	180 Hz	190 Hz
f_H	1.1 MHz	1.3 MHz

The output resistance of the current source is made larger if there's an emitter resistor. Therefore, the 220-Ω resistor in our circuit helps to increase the current source output resistance. If $R_E > r_\pi$, the output resistance approaches $r_\mu/2$, which is a very large value. At the bias levels chosen, component values are $g_{m2} = 0.1$, $r_{\pi2} = 1750$ Ω, $r_{o2} = 54$ kΩ, and $r_{\mu2} = 9.4$ MΩ. The output resistance $r_{out2} \approx 900$ kΩ.

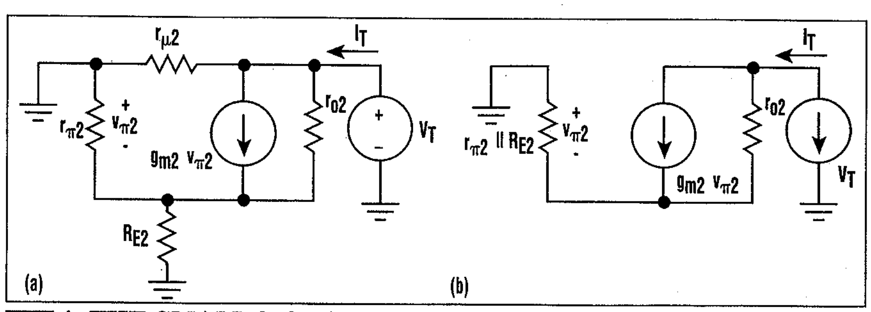
The final step is to find the input resistance of the emitter follower *(Fig. 5)*. The resistance looking into the base of Q_3 (the derivation of which is left as an exercise for the reader) is given by:

$$r_{in3} = r_{\mu3} \| \{r_{\pi3} + (1 + h_{fe3})(r_{o3} \| R_{E3})\} \quad (20)$$

With $R_{E3} = 10$ kΩ, Q_3 is biased at approximately 1.5 mA, resulting in: $g_{m3} = 0.06$, $r_{\pi3} = 3.3$ kΩ, $r_{o3} = 250$ kΩ, and $r_{\mu3} = 50$ MΩ. This results in $r_{in3} \approx 2$ MΩ.

Because r_{o1} is the smallest of the three resistors at the output node, it's the limiting factor in the amplifier's open-loop gain. The sum of the three equivalent resistors in parallel results in a resistance of approximately 114 kΩ between the high-gain node and ground. From Equation 14, the open-loop gain is approximately -11,400. This gain is high enough so that when the loop is closed, the amplifier's gain should approach the ideal gain.

If the gain is now acceptable, what about the bandwidth? If we assume that there's one dominant pole (that pole being due to the Miller capacitance of Q_1), and that all other poles are at frequencies much higher than 1 MHz, the gain-bandwidth product of the amplifier will be constant. In order for our amplifier with closed-loop gain



4. THE SMALL-SIGNAL MODEL of the current source Q_2 is used to find its output resistance (a). At first this circuit looks complicated, but it's possible to simplify it by omitting $r_{\mu2}$ (b).

of –1000 to have a –3-dB bandwidth of 1 MHz, the open-loop bandwidth must be at least 90 kHz (at a gain of 11,400). The dominant pole of this amplifier is due to the effective source resistance ($R_{in} + r_{x1}$) interacting with the Miller capacitance *(see "The Miller approximation," p. 86)*. Other poles (for instance, in the emitter follower Q_3) will be at much higher frequencies. This can be seen by applying the method of Open-Circuit Time Constants to the amplifier.[4,5] Using the Miller approximation, and assuming $a_v = 11{,}400$, $C_{\mu1} = 2$ pF, $r_{\pi1} = 2$ kΩ, $r_{x1} = 150$ Ω, and $R_{in} = 85$ Ω, the open-loop –3-dB bandwidth is given by:

$$f_H \approx \frac{1}{2\pi\{(R_{in} + r_{x1})\|r_{\pi1}\}a_v C_{\mu1}} \approx 33 \text{ kHz} \quad (21)$$

The Miller approximation tells us that at a gain of 1000, the closed loop bandwidth won't be much larger than 380 kHz. Measurements on the breadboard prototype and Spice results confirm this prognosis *(Table 4)*. The Miller effect is killing us!

What can be done to squeeze more bandwidth out of the circuit? Because the Miller effect is hurting us, let's overcome it by using a cascode transistor *(Fig. 6)*. With the added cascode transistor Q_5, the gain at the collector of Q_1 is low because transistor Q_5 has a small output resistance at its emitter. This defeats the Miller effect by isolating the high gain node from the input transistor Q_1. The input capacitance of Q_1 is now much lower (approximately $C_{\pi1} + 2C_{\mu1}$), moving the input pole up to a frequency given by:

$$f_{input\_pole} \approx \frac{1}{2\pi\{r_{\pi1}\|(R_{in} + r_{x1})\}(C_{\pi1} + 2C_{\mu1})} \approx 14 \text{ MHz} \quad (22)$$

This amplifier's dominant time constant will be the resistance of the high-gain node (now higher than 114 kΩ, due to the cascode transistor) interacting with the various capacitances at the node. All other poles will be at frequencies much higher than our closed-loop bandwidth of 1 MHz. The modified circuit also will have a higher open-loop gain, because the cascode transistor reduces the effects of base-width modulation on transistor Q_1.

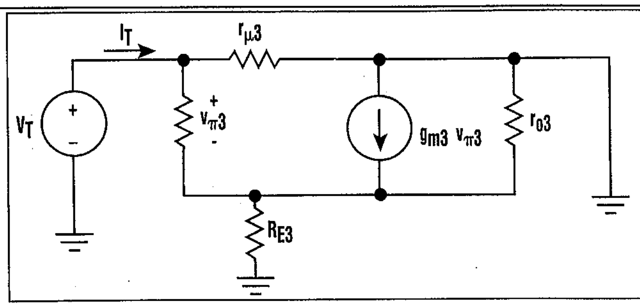
Now, let's do a non-rigorous, seat-of-the-pants calculation. Because Q_5 has a high impedance at its emitter, the output resistance at the collector of the cascode transistor will be approximately $r_{\mu5}/2$ *(see Equation 18)*. Consequently, the equivalent resistance r_{eq} at the high-gain node now is approximately equal to the output resistance of the current source r_{out2} in parallel with the input resistance of the emitter follower. This resistance $r_{eq} \approx 600$ kΩ. Therefore, the open-loop gain ($\approx -g_{m1}r_{eq}$) $\approx -60{,}000$.

$C_{\mu2}$ will be slightly larger than in the previous circuit, because V_{CB2} is smaller with the added cascode transistor. There's no Miller effect, so the total capacitance C_T at the high-gain node is approximately $C_T = C_{\mu5} + C_{\mu2} + C_{\mu3}$ + stray capacitances ≈ 10 pF. Given this, the dominant open-loop pole is approximately:

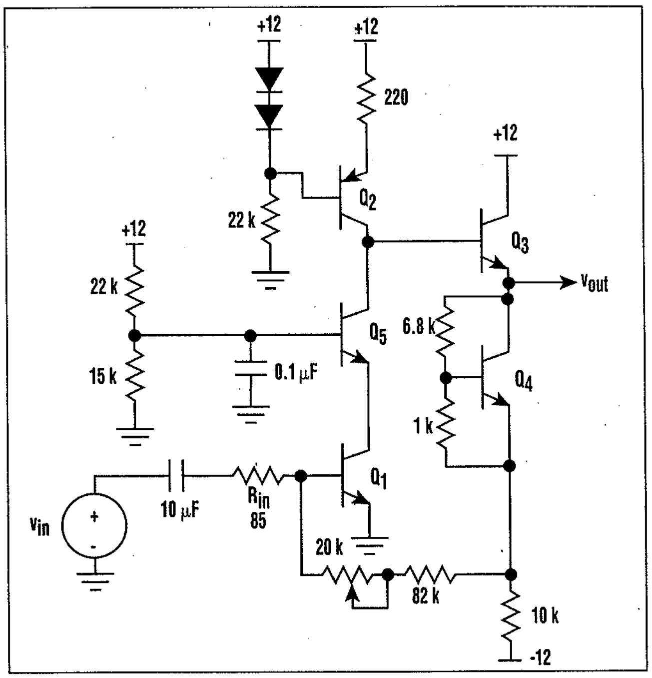
$$f_{OL} \approx \frac{1}{2\pi\, r_{eq} C_T} \approx 26 \text{ kHz} \quad (23)$$

The poles are widely spaced, so the feedback loop should be stable and with a bandwidth 60 times larger than the dominant open-loop pole ≈ 1.6 MHz. We expect the actual bandwidth to be lower, and measurements show that it is, due to other unexplained effects *(Table 5)*.

Finally, the bandwidth specifications have been met. This article demonstrates that it's possible to design a simple, high-gain amplifier with wide bandwidth. To reiterate, the approach used was designed to emphasize intuition, not analytical results. □



5. ENGINEERS CAN calculate the input resistance of the emitter follower using the circuit's small-signal model.



6. ADDING A CASCODE transistor will eradicate the Miller effect and squeeze more bandwidth out of the single-stage high-gain amplifier circuit.

Marc Thompson is a senior engineer at Polaroid's Medical Imaging Systems, where he specializes in high-speed analog design. He has two patents for the design of high-speed, high-power laser diode modulators. Marc holds a BSEE and MSEE from the Massachusetts Institute of Technology, Cambridge, and is currently on a leave-of-absence from Polaroid pursuing his PhD at MIT.

This article is fourth in a series of Marc's analog design articles that have run in Electronic Design over the past year. The four articles are based on his analog-design seminar that's offered at Polaroid.

References:

1. Roberge, James K., *Operational Amplifiers: Theory and Practice,*

DESIGN APPLICATIONS

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John Wiley and Sons: New York, 1975, p. 309-326.

2. Early, James, "Effects of Space-Charge Layer Widening in Junction Transistors," Proceedings of the I.R.E., November 1952, p. 1401-1406.

3. Thompson, Marc, "SCTC Analysis Estimates Low-Frequency –3-dB Point," *Electronic Design*, October 1, 1993, p. 65-68.

4. Thompson, Marc, "Design Linear Circuits Using OCTC Calculations," *Electronic Design Special Analog Issue*, June 24, 1993, p. 41-47.

5. Thompson, Marc, "Network Tricks Aid in OCTC," *Electronic Design*, December 16, 1993, p. 67-70.

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555